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Preliminary *1M X 18, 512K X 36 LVTTL, Flow-through ZeBL™ SRAM*

Document Title

1M X 18, 512K X 36 LVTTL, Flow-through ZeBL™ SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	August, 20, 2005	Preliminary

Preliminary 1M X 18, 512K X 36 LVTTL, Flow-through ZeBL™ SRAM

Features

- Fast access time: 6.5/7.5/8.5 ns (153, 133, 117 MHz)
- Zero Bus Latency between READ and WRITE cycles allows 100% bus utilization
- Signal +3.3V ± 5% power supply
- Individual Byte Write control capability
- Clock enable ($\overline{CEN}$) pin to enable clock and suspend operations
- Clock-controlled and registered address, data and control signals
- Registered output for pipelined applications
- Three separate chip enables allow wide range of options for CE control, address pipelining
- Internally self-timed write cycle
- Selectable BURST mode (Linear or Interleaved)
- SLEEP mode (ZZ pin) provided
- Available in 100 pin LQFP package

General Description

The AMIC Zero Bus Latency (ZeBL™) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

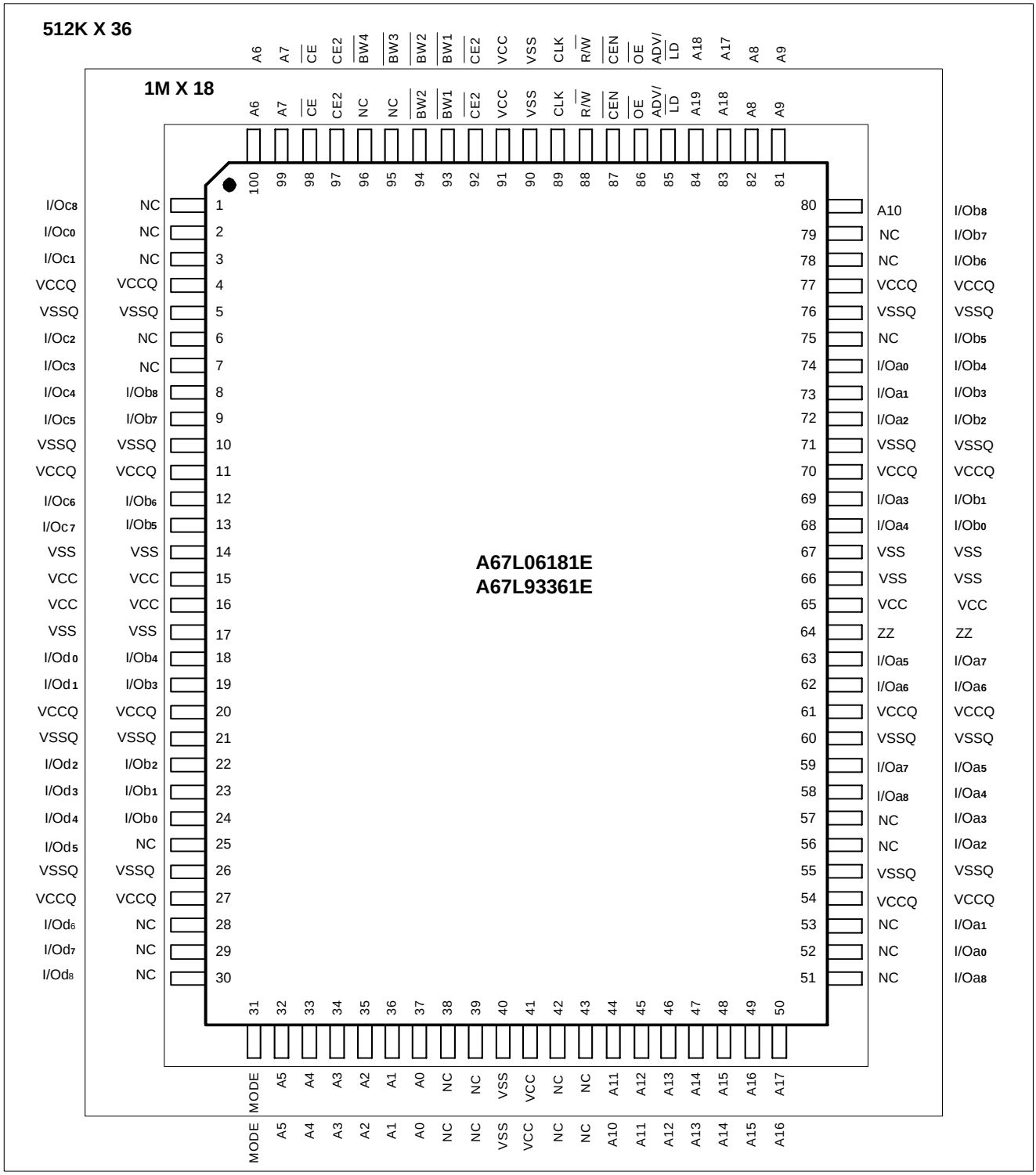
The A67L06181, A67L93361 SRAMs integrate a 1M X 18, 512K X 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization without the insertion of any wait cycles during Write-Read alternation. The positive edge triggered single clock input (CLK) controls all synchronous inputs passing through the registers. The synchronous inputs include all address, all data inputs, active low chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), cycle start input (ADV/$\overline{LD}$), synchronous clock enable ($\overline{CEN}$), byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and read/write (R/$\overline{W}$).

Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK), SLEEP mode (ZZ, tied LOW if unused) and burst mode (MODE). Burst Mode can provide either interleaved or linear operation, burst operation can be initiated by synchronous address Advance/Load (ADV/$\overline{LD}$) pin in Low state. Subsequent burst address can be internally generated by the chip and controlled by the same input pin ADV/$\overline{LD}$ in High state.

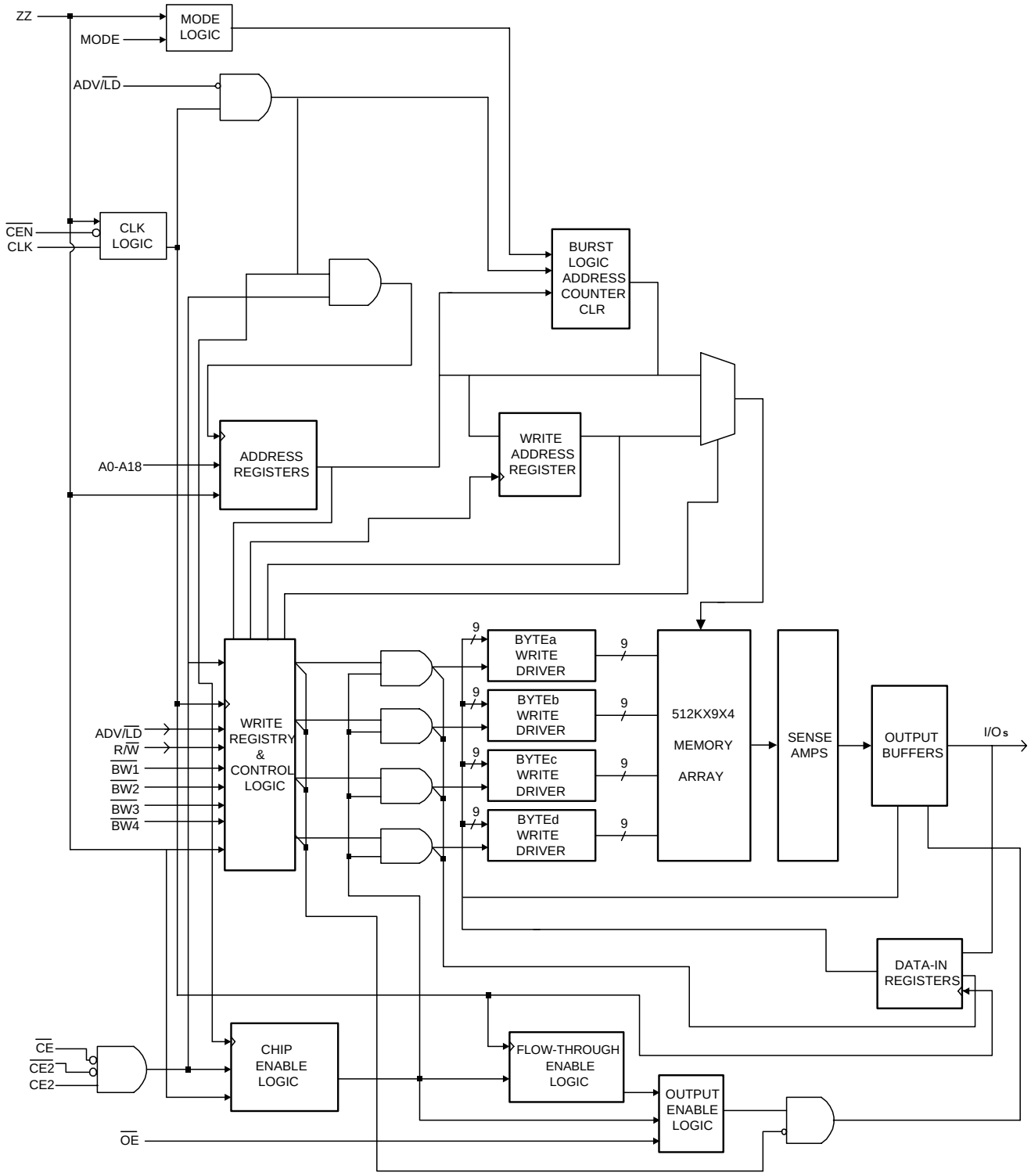
Write cycles are internally self-time and synchronous with the rising edge of the clock input and when R/$\overline{W}$ is Low. The feature simplified the write interface. Individual Byte enables allow individual bytes to be written. $\overline{BW1}$ controls I/Oa pins; $\overline{BW2}$ controls I/Ob pins; $\overline{BW3}$ controls I/Oc pins; and $\overline{BW4}$ controls I/Od pins. Cycle types can only be defined when an address is loaded.

The SRAM operates from a +3.3V power supply, and all inputs and outputs are LVTTL-compatible. The device is ideally suited for high bandwidth utilization systems.

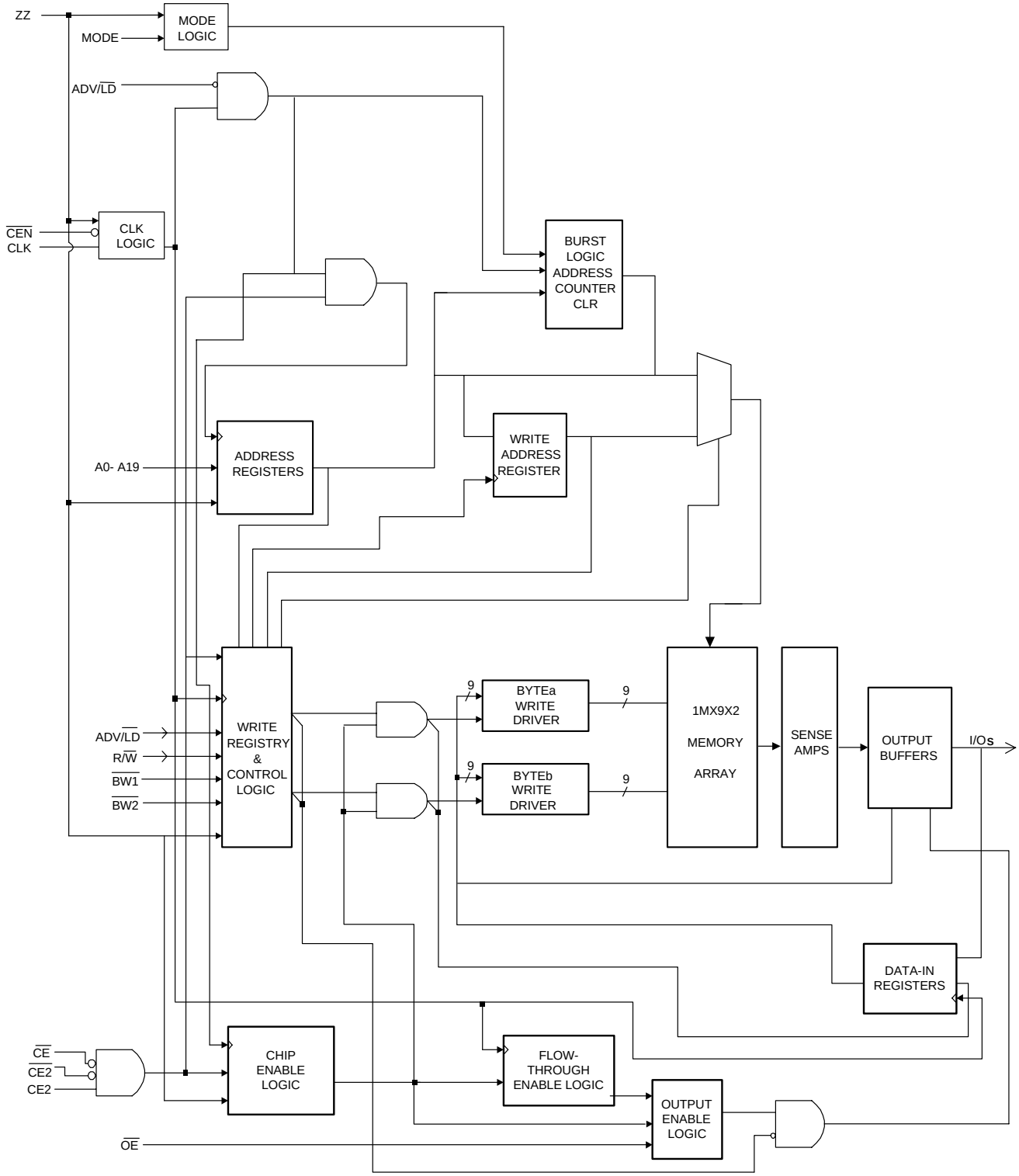
Pin Configuration


512K X 36
1M X 18
A67L06181E
A67L93361E
100 A6 | NC I/Oc8
99 A7 | NC I/Oc0
98 CE | NC I/Oc1
97 CE2 | VCCQ VCCQ
96 NC | VSSQ VSSQ
95 NC | NC I/Oc2
94 BW2 | NC I/Oc3
93 BW1 | I/Ob8 I/Oc4
92 CE2 | I/Ob7 I/Oc5
91 VCC | VSSQ VSSQ
90 VSS | VCCQ VCCQ
89 CLK | I/Ob6 I/Oc6
88 R/W | I/Ob5 I/Oc7
87 CEN | VSS VSS
86 OE | VCC VCC
85 ADV/LD | VCC VCC
84 A19 | VSS VSS
83 A18 | I/Ob4 I/Od0
82 A8 | I/Ob3 I/Od1
81 A9 | VCCQ VCCQ
80 A10 | I/Ob8 I/Od2
79 NC | I/Ob7 I/Od3
78 NC | I/Ob6 I/Od4
77 VCCQ | VCCQ I/Od5
76 VSSQ | VSSQ VSSQ
75 NC | I/Ob5 I/Od6
74 I/Oa0 | I/Ob4 I/Od7
73 I/Oa1 | I/Ob3 I/Od8
72 I/Oa2 | I/Ob2 NC
71 VSSQ | VSSQ VSSQ
70 VCCQ | VCCQ VCCQ
69 I/Oa3 | I/Ob1 NC
68 I/Oa4 | I/Ob0 NC
67 VSS | VSS VSS
66 VSS | VSS VSS
65 VCC | VCC VCC
64 ZZ | ZZ NC
63 I/Oa5 | I/Oa7 NC
62 I/Oa6 | I/Oa6 NC
61 VCCQ | VCCQ VCCQ
60 VSSQ | VSSQ VSSQ
59 I/Oa7 | I/Oa5 NC
58 I/Oa8 | I/Oa4 NC
57 NC | I/Oa3 NC
56 NC | I/Oa2 NC
55 VSSQ | VSSQ VSSQ
54 VCCQ | VCCQ VCCQ
53 NC | I/Oa1 NC
52 NC | I/Oa0 NC
51 NC | I/Oa8 NC
1 MODE | MODE
2 A5 | A5
3 A4 | A4
4 A3 | A3
5 A2 | A2
6 A1 | A1
7 A0 | A0
8 NC | NC
9 NC | NC
10 VSS | VSS
11 VCC | VCC
12 NC | NC
13 NC | NC
14 A11 | A10
15 A12 | A11
16 A13 | A12
17 A14 | A13
18 A15 | A14
19 A16 | A15
20 A17 | A16

Block Diagram (512K X 36)



Block Diagram (1M X 18)



Pin Description

Pin No.		Symbol	Description
LQFP (X18)	LQFP (X36)		
37 36 35,34,33,32, 100,99,82,81 44,45,46,47, 48,49,50,83 84 80	37 36 35,34,33,32, 100,99,82,81 45,46,47,48, 49,50,83,84 44	A0 A1 A2 – A9 A11-A18 A19 A10	Synchronous Address Inputs : These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pins 83 and 84 are reserved as address bits for higher-density 9Mb and 18Mb DBA SRAMs, respectively. A0 and A1 are the two lest significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 ($\overline{BW1}$) 94 ($\overline{BW2}$)	93 ($\overline{BW1}$) 94 ($\overline{BW2}$) 95 ($\overline{BW3}$) 96 ($\overline{BW4}$)	$\overline{BW1}$ $\overline{BW2}$ $\overline{BW3}$ $\overline{BW4}$	Synchronous Byte Write Enables : These active low inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address, $\overline{BWs}$ are associated with addresses and apply to subsequent data. $\overline{BW1}$ controls I/Oa pins; $\overline{BW2}$ controls I/Ob pins; $\overline{BW3}$ controls I/Oc pins; $\overline{BW4}$ controls I/Od pins.
89	89	CLK	Clock : This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	$\overline{CE}$	Synchronous Chip Enable : This active low input is used to enable the device. This input is sampled only when a new external address is loaded (ADV/$\overline{LD}$ LOW).
92	92	$\overline{CE2}$	Synchronous Chip Enable : This active low input is used to enable the device and is sampled only when a new external address is loaded (ADV/$\overline{LD}$ LOW). This input can be used for memory depth expansion.
97	97	CE2	Synchronous Chip Enable : This active high input is used to enable the device and is sampled only when a new external address is loaded (ADV/$\overline{LD}$ LOW). This input can be used for memory depth expansion.
86	86	$\overline{OE}$	Output Enable : This active low asynchronous input enables the data I/O output drivers.
85	85	ADV/$\overline{LD}$	Synchronous Address Advance/Load : When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When HIGH, R/$\overline{W}$ is ignored. A LOW on this pin permits a new address to be loaded at CLK rising edge.
87	87	$\overline{CEN}$	Synchronous Clock Enable : This active low input permits CLK to propagate throughout the device. When HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.

Pin Description (continued)

Pin No.		Symbol	Description
LQFP (X18)	LQFP (X36)		
64	64	ZZ	Snooze Enable : This active high asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored.
88	88	R/$\overline{W}$	Read/Write : This active input determines the cycle type when ADV/$\overline{LD}$ is LOW. This is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus width WRITEs occur if all byte write enables are LOW.
74, 73, 72, 69, 68 63, 62, 59, 58 24, 23, 22, 19, 18 13, 12, 9, 8	52, 53, 56, 57, 58, 59, 62, 63, 51 68, 69, 72, 73, 74, 75, 78, 79, 80 2, 3, 6, 7, 8, 9, 12, 13,1 18, 19, 22, 23, 24, 25, 28, 29, 30	I/Oa I/Ob I/Oc I/Od	SRAM Data I/O : Byte “a” is I/Oa pins; Byte “b” is I/Ob pins; Byte “c” is I/Oc pins; Byte “d” is I/Od pins. Input data must meet setup and hold times around CLK rising edge.
31	31	MODE	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating.
1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42,43 51, 52, 53, 56, 57, 75, 78, 79, 95, 96	38,39,42,43	NC	No Connect : These pins can be left floating or connected to GND to minimize thermal impedance.
15, 16, 41, 65, 91	15, 16, 41, 65, 91	VCC	Power Supply
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	VCCQ	Isolated Output Buffer Supply
14, 17, 40, 66, 90	14, 17, 40, 66, 90	VSS	Ground : GND.
5,10,21,26, 55,60,71,76	5,10,21,26, 55,60,71,76	VSSQ	Isolated Output Buffer Ground

Truth Table (Notes 5 - 7)

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	ADV/$\overline{LD}$	R/$\overline{W}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CEN}$	CLK	I/O	Notes
Deselected Cycle, Power-down	None	H	X	X	L	L	X	X	X	L	L→H	High-Z	
Deselected Cycle, Power-down	None	X	H	X	L	L	X	X	X	L	L→H	High-Z	
Deselected Cycle, Power-down	None	X	X	L	L	L	X	X	X	L	L→H	High-Z	
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L→H	High-Z	1
READ Cycle (Begin Burst)	External	L	L	H	L	L	H	X	L	L	L→H	Q	
READ Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L→H	Q	1,7
NOP/Dummy READ (Begin Burst)	External	L	L	H	L	L	H	X	H	L	L→H	High-Z	2
Dummy READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L→H	High-Z	1,2,7
WRITE Cycle (Begin Burst)	External	L	L	H	L	L	L	L	X	L	L→H	D	3
WRITE Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L→H	D	1,3,7
NOP/WRITE Abort (Begin Burst)	None	L	L	H	L	L	L	H	X	L	L→H	High-Z	2,3
WRITE Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L→H	High-Z	1,2,3,7
IGNORE Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L→H	-	4
SLEEP Mode	None	X	X	X	H	X	X	X	X	X	X	High-Z	

Notes:

1. Continue Burst cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial Begin Burst cycle. A Continue Deselect cycle can only be entered if a Deselect cycle is executed first.
2. Dummy READ and WRITE Abort cycles can be considered NOPs because the device performs no operation. A WRITE Abort means a WRITE command is given, but no operation is performed.
3. $\overline{OE}$ may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. Some users may use $\overline{OE}$ when the bus turn-on and turn-off times do not meet their requirements.
4. If an Ignore Clock Edge command occurs during a READ operation, the I/O bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the Ignored Clock Edge cycle.
5. X means "Don't Care." H means logic HIGH. L means logic LOW. $\overline{BWx}$ = H means all byte write signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ and $\overline{BW4}$) are HIGH. $\overline{BWx}$ = L means one or more byte write signals are LOW.
6. $\overline{BW1}$enables WRITEs to Byte "a" (I/Oa pins); $\overline{BW2}$ enables WRITEs to Byte "b" (I/Ob pins); $\overline{BW3}$ enables WRITEs to Byte "c" (I/Oc pins); $\overline{BW4}$ enables WRITEs to Byte "d" (I/Od pins).
7. The address counter is incremented for all Continue Burst cycles.

Partial Truth Table for READ/WRITE Commands (X18)

Operation	R/$\overline{W}$	$\overline{BW1}$	$\overline{BW2}$
READ	H	X	X
WRITE Byte “a”	L	L	H
WRITE Byte “b”	L	H	L
WRITE all bytes	L	L	L
WRITE Abort/NOP	L	H	H

Note : Using R/$\overline{W}$ and BYTE WRITE(s), any one or more bytes may be written.

Partial Truth Table for READ/WRITE Commands (X36)

Operation	R/$\overline{W}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	X	X	X	X
WRITE Byte “a”	L	L	H	H	H
WRITE Byte “b”	L	H	L	H	H
WRITE Byte “c”	L	H	H	L	H
WRITE Byte “d”	L	H	H	H	L
WRITE all bytes	L	L	L	L	L
WRITE Abort/NOP	L	H	H	H	H

Note : Using R/$\overline{W}$ and BYTE WRITE(s), any one or more bytes may be written.

Linear Burst Address Table (MODE = LOW)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

Interleaved Burst Address Table (MODE = HIGH or NC)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

Absolute Maximum Ratings*

Power Supply Voltage (VCC) . . . . . -0.3V to +4.6V
Voltage Relative to GND for any Pin Except VCC (Vin, Vout) . . . . . -0.3V to VCC +0.3V
Operating Temperature (Topr) . . . . . 0°C to 70°C
Storage Temperature (Tbias) . . . . . -10°C to 85 °C
Storage Temperature (Tstg) . . . . . -55°C to 125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics and Operating Conditions

(0°C ≤ T_A ≤ 70°C, VCC, VCCQ = +3.3V± 5% unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Max.	Unit	Note
V_{IH}	Input High Voltage		1.7	VCC+0.3	V	1,2
V_{IL}	Input Low Voltage		-0.3	0.8	V	1,2
I_{LI}	Input Leakage Current	0V ≤ V_{IH} ≤ VCC	-2.0	2.0	μA	
I_{LO}	Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN}≤ VCC	-2.0	2.0	μA	
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.0		V	1,3
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA		0.4	V	1,3
VCC	Supply Voltage		3.135	3.465	V	1
VCCQ	Isolated Output Buffer Supply		3.135	VCC	V	1,4

Capacitance

Symbol	Parameter	Conditions	Typ.	Max.	Unit	Note
C_I	Control Input Capacitance	T_A = 25°C; f = 1MHz	3	4	pF	6
C_O	Input/Output Capacitance (I/O)	VCC = 3.3V	4	5	pF	6
C_A	Address Capacitance		3	3.5	pF	6

Note : 1. All voltages referenced to VSS (GND).
2. Overshoot : V_{IH} ≤ +4.6V for t ≤ t_{KHKH}/2 for I ≤ 20mA
Undershoot : V_{IL} ≥ -0.7V for t ≤ t_{KHKH}/2 for I ≤ 20mA
Power-up : V_{IH} ≤ +3.465V and VCC ≤ 3.135V for t ≤ 200ms
3. The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
4. VCC and VCCQ can be externally wired together to the same power supply.
5. This parameter is sampled.

I_{CC} Operating Condition and Maximum Limits

Symbol	Parameter	Max.			Unit	Conditions
		-7.5	-8.5	-10.0		
I_{CC}	Power Supply Current : Operating	TBD	TBD	TBD	mA	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ t_{KC} (MIN); VCC = MAX; Output open
I_{SB}	Standby	TBD	TBD	TBD	mA	Device deselected; VCC = MAX; All inputs ≤ VSS+0.2 or ≥ VCC-0.2; Cycle time ≥ t_{KC} (MIN)
I_{SB}	Standby	TBD	TBD	TBD	mA	Device deselected; VCC = MAX; All inputs ≤VSS+0.2 or ≥ VCC-0.2; All inputs static; CLK frequency=MAX; ZZ ≥ V_{CC}-0.2V
I_{SB2}	Standby	TBD	TBD	TBD	mA	Device deselected; VCC = MAX; All inputs ≤ V_{IL}; or ≥ V_{IH}; All inputs static; CLK frequency=0
I_{SB2Z}	SLEEP Mode	TBD	TBD	TBD	mA	ZZ ≥ V_{IH}

AC Characteristics (Note 4)

($0°C \le T_A \le 70°C$, VCC = +3.3V± 5%)

Symbol	Parameter	-7.5		-8.5		-10.0		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Clock									
t_{KHKH}	Clock cycle time	7.5	-	-8.5	-	10	-	ns	
t_{KF}	Clock frequency	-	133	-	117	-	100	MHz	
t_{KHKL}	Clock HIGH time	2.5	-	2.8	-	3.0	-	ns	
t_{KLKH}	Clock LOW time	2.5	-	2.8	-	3.0	-	ns	
Output Times									
t_{KHQV}	Clock to output valid	-	6.5	-	7.5	-	8.5	ns	
t_{KHQX}	Clock to output invalid	3.0	-	3.0	-	3.0	-	ns	
t_{KHQX1}	Clock to output in Low-Z	2.5	-	2.5	-	2.5	-	ns	1,2,3
t_{KHQZ}	Clock to output in High-Z	1.5	3.8	1.5	4.0	1.5	5.0	ns	1,2,3
t_{GLQV}	$\overline{OE}$ to output valid	-	3.5	-	3.5	-	4.0	ns	4
t_{GLQX}	$\overline{OE}$ to output in Low-Z	0	-	0	-	0	-	ns	1,2,3
t_{GHQZ}	$\overline{OE}$ to output in High-Z	-	3.5	-	3.5	-	4.0	ns	1,2,3
Setup Times									
t_{AVKH}	Address	1.5	-	2.0	-	2.0	-	ns	5
t_{EVKH}	Clock enable ($\overline{CEN}$)	1.5	-	2.0	-	2.0	-	ns	5
t_{CVKH}	Control signals	1.5	-	2.0	-	2.0	-	ns	5
t_{DVKH}	Data-in	1.5	-	2.0	-	2.0	-	ns	5
Hold Times									
t_{KHAX}	Address	0.5	-	0.5	-	0.5	-	ns	5
t_{KHEX}	Clock enable ($\overline{CEN}$)	0.5	-	0.5	-	0.5	-	ns	5
t_{KHCX}	Control signals	0.5	-	0.5	-	0.5	-	ns	5
t_{KHDX}	Data-in	0.5	-	0.5	-	0.5	-	ns	5

Notes: 1. This parameter is sampled.

2. Output loading is specified with C1=5pF as in Figure 2.
3. Transition is measured ±200mV from steady state voltage.
4. $\overline{OE}$ can be considered a “Don’t Care” during WRITE; however, controlling $\overline{OE}$ can help fine-tune a system for turnaround timing.
5. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when ADV/$\overline{LD}$ is LOW and chip enabled. All other synchronous inputs meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when ADV/$\overline{LD}$ is LOW) to remain enabled.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.0ns
Input Timing Reference Levels	1.25V
Output Reference Levels	1.25V
Output Load	See Figures 1 and 2

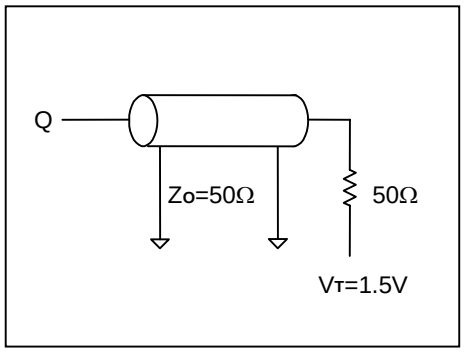


Figure 1
Output Load Equivalent

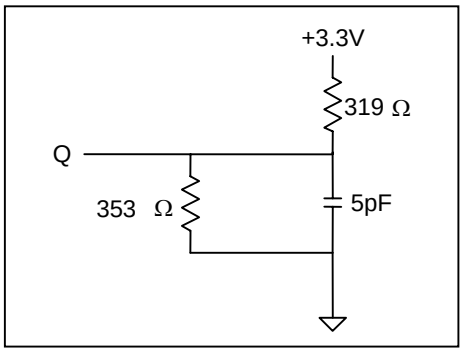


Figure 2
Output Load Equivalent

SLEEP Mode

SLEEP Mode is a low current “Power-down” mode in which the device is deselected and current is reduced to I_{SB2Z}. This duration of SLEEP Mode is dictated by the length of time the ZZ is in a HIGH state. After entering SLEEP Mode, all inputs except ZZ become disabled and all outputs go to High-Z.
The ZZ pin is asynchronous, active high input that causes the device to enter SLEEP Mode. When the ZZ pin becomes logic HIGH, ISB2Z is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP Mode is not guaranteed to successfully complete. Therefore, SLEEP Mode (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP Mode during t_{RZZ}, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP Mode.

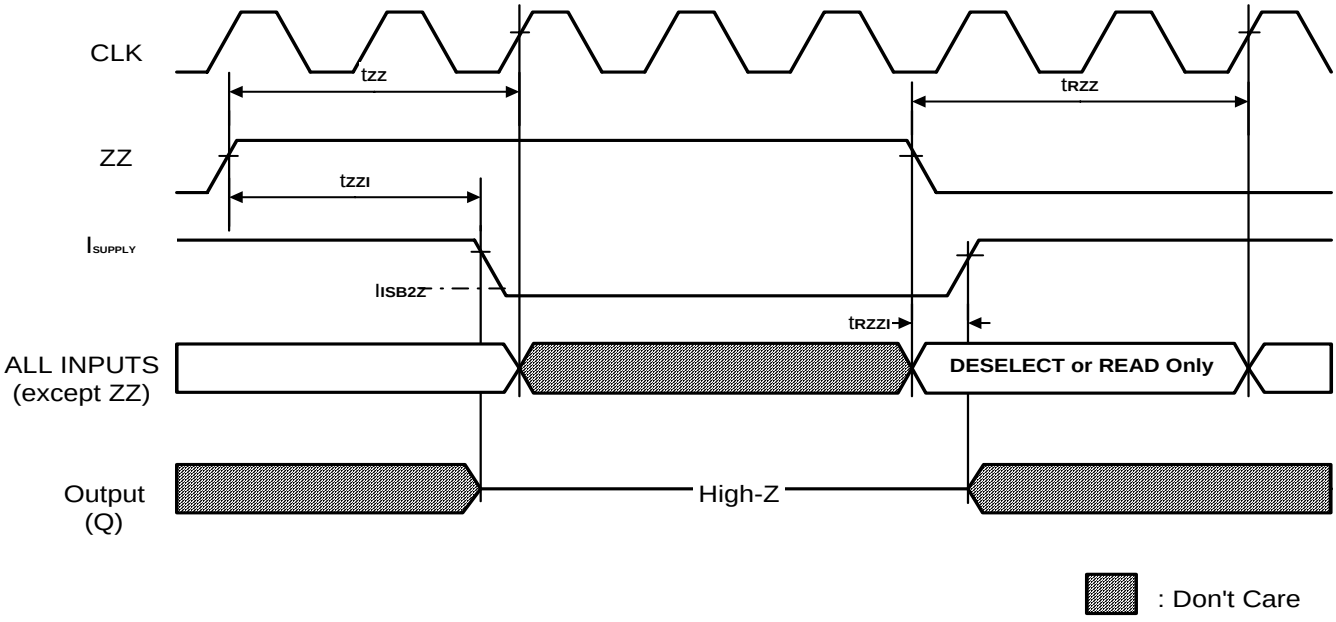
SLEEP Mode Electrical Characteristics

(VCC, VCCQ = +3.3V±5%)

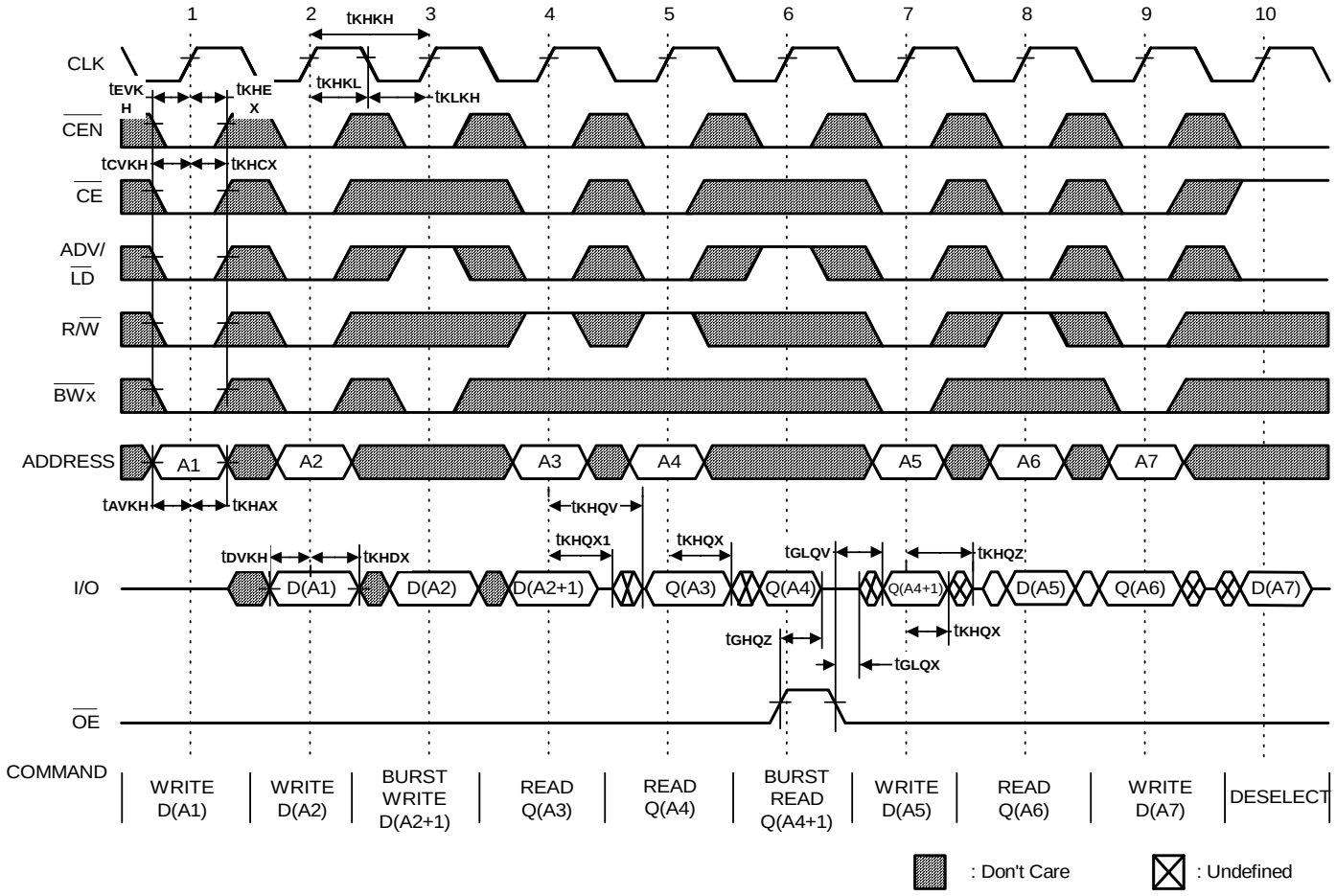
Symbol	Parameter	Conditions	Min.	Max.	Unit	Note
I_{SB2Z}	Current during SLEEP Mode	ZZ ≥ V_{IH}	-	TBD	mA	
t_{ZZ}	ZZ active to input ignored		0	2(t_{KHKH})	ns	1
t_{RZZ}	ZZ inactive to input sampled		0	2(t_{KHKH})	ns	1
t_{ZZI}	ZZ active to snooze current		-	2(t_{KHKH})	ns	1
t_{RZZI}	ZZ inactive to exit snooze current		0		ns	1

Note : 1. This parameter is sampled.

SLEEP Mode Waveform



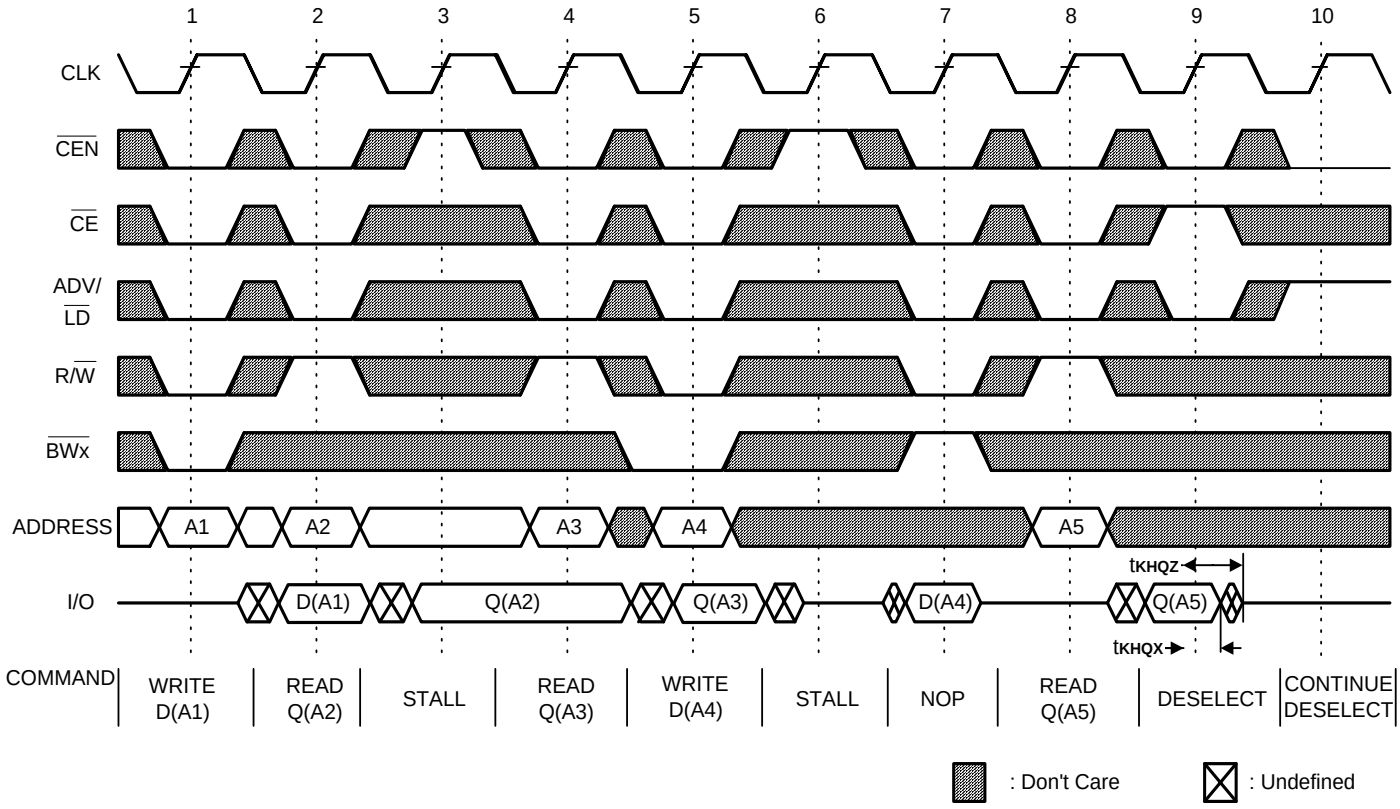
READ/WRITE Timing



Note : 1. For this waveform, ZZ is tied LOW.

2. Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BRST operations are optional.
3. $\overline{CE}$ represents three signals. When $\overline{CE}$ = 0, it represents $\overline{CE}$ = 0, $\overline{CE2}$ = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated the most current data is used. The most recent data may be from the input data register.

NOP, STALL and Deselect Cycles



Note : 1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates $\overline{CEN}$ being used to create a "pause." A WRITE is not performed during this cycle.

2. For this waveform, ZZ and $\overline{OE}$ are tied LOW.
3. $\overline{CE}$ represents three signals. When $\overline{CE}$ = 0, it represents $\overline{CE}$ = 0, $\overline{CE2}$ = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

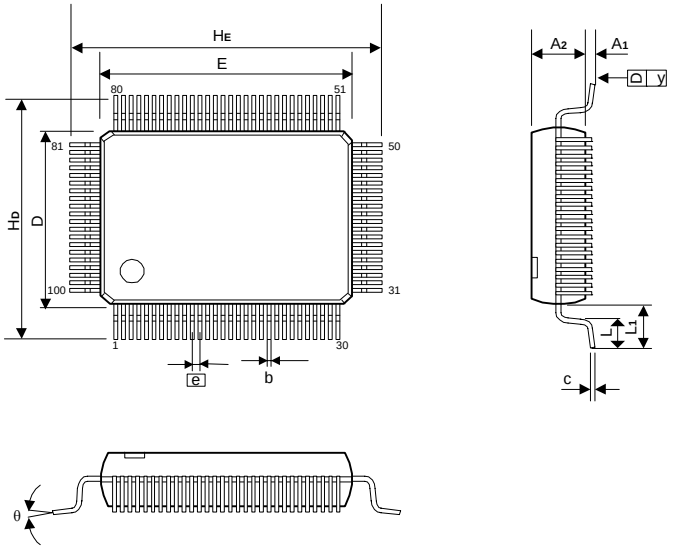
Ordering Information

Part No.	Configure	Cycle Time / Access Time	Package
A67L06181E-7.5	1M X 18	7.5ns / 6.5ns	100L LQFP
A67L06181E-7.5F		7.5ns / 6.5ns	100L Pb-Free LQFP
A67L06181E-8.5		8.5ns / 7.5ns	100L LQFP
A67L06181E-8.5F		8.5ns / 7.5ns	100L Pb-Free LQFP
A67L06181E-10.0		10ns / 8.5ns	100L LQFP
A67L06181E-10.0F		10ns / 8.5ns	100L Pb-Free LQFP
A67L93361E-7.5	512K X 36	7.5ns / 6.5ns	100L LQFP
A67L93361E-7.5F		7.5ns / 6.5ns	100L Pb-Free LQFP
A67L93361E-8.5		8.5ns / 7.5ns	100L LQFP
A67L93361E-8.5F		8.5ns / 7.5ns	100L Pb-Free LQFP
A67L93361E-10.0		10ns / 8.5ns	100L LQFP
A67L93361E-10.0F		10ns / 8.5ns	100L Pb-Free LQFP

Package Information

LQFP 100L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.009	0.012	0.015	0.22	0.30	0.38
c	0.004	-	0.008	0.09	-	0.20
H_E	0.866 BSC			22.00 BSC		
E	0.787 BSC			20.00 BSC		
H_D	0.630 BSC			16.00 BSC		
D	0.551 BSC			14.00 BSC		
e	0.026 BSC			0.65 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.